Form PTO-1449 (REV. 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty. Docket No. 13647A (BUR20000082US2)	Serial No. 10/801387 ~~Unassigned~~
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
VN	AA	5,945,834	8/31/99	Nakata, et al.			
	AB	5,898,629	4/27/99	Beffa, et al.			
	AC	5,831,445	11/3/98	Atkins, et al.			
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OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

VN		"WAFER LEVEL TEST AND BURN IN", IBM Technical Disclosure Bulletin, January 1992, pp. 401-404;
VN		"MULTI-LAYER CERAMIC SPACE TRANSFORMER FOR WAFER LEVEL STRESS", IBM Technical Disclosure Bulletin, April 1999, pp. 385 - 386;
VN		"WAFER BURN-IN ISOLATION CIRCUIT", IBM Technical Disclosure Bulletin, November 1989, pp. 442-443

EXAMINER Minh Nguyen DATE CONSIDERED 10/14/06

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